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SG Undersea Cable System:

Semiconductor Devices and Passive Components

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In this paper we describe the active devices and passive components used in the SG undersea cable system for the TAT-6 link between Green Hill, Rhode Island, and St. Hilaire de Riez, France. We explain reasons for component choice and present information about design, performance, screening, and reliability.

I. INTRODUCTION

Traditionally, in high-reliability communication systems such as undersea telephone cables, well-established component and device designs and manufacturing processes are used. But with the development of the SG undersea cable system, this conservative approach has been challenged by the need for devices of higher performance. This requirement resulted, in some cases, in sophisticated device designs that border on "state-of-the-art" concepts. For example, the increase in channel capacity or bandwidth requires high-frequency transistors incorporating design and processing features that are relatively new. Nevertheless, new features were carefully evaluated so that they would meet the system reliability requirements. In general, reliability is the governing criterion for the selection of components and devices for the undersea cable system. This concept and how it applies to passive components and active devices are covered in the following subsections: II, transistors; III, diodes; IV, gas tubes; V, resistors; VI, capacitors; and VII, inductors and transformers. Each subsection is complete for each component or device and covers: (*i*) choice and requirements, (*ii*) design and construction, (*iii*) characterization and screening, and (*iv*) aging.

II. TRANSISTORS

2.1 Requirements

Although there are seven transistor codes, six in each repeater, all are the same basic design. This, of course, is a very desirable arrangement for simplicity and economy of manufacture. The basic development code is a passivated npn silicon planar transistor and is divided into: (*i*) the 82A for the input stage, selected chiefly for low noise; (*ii*) the 82B and 82C as intermediate-stage devices selected for high gain and low capacitance, respectively; (*iii*) the 82D and 82E as driver and output transistors, which are optimized for low second- and low third-order modulation coefficients, respectively; and (*iv*) the 82F and 82G for low- and high-band oscillators. Table I shows assignment of the transistor codes to the various functions and their most critical characteristics.

2.2 Design

The design of the transistor draws on the epitaxial, planar, and noble contact metallurgy technology commonly used in contemporary discrete and integrated devices.

2.2.1 Thermal considerations

Being a power high-frequency transistor, the transistor's active element is in essence an array of conventional, small, high-frequency devices electrically connected in parallel on the same silicon chip. Packing a large number of these small devices close together (to keep capacitance low) naturally creates a thermal problem. And where both reliability and low distortion performance are important, this problem becomes critical. For a long service life, the transistor must operate at as low a temperature as possible, and at the same time all parts of the active element must be

Table I — Location and characteristics of transistors

Transistor Code	Circuit Designation	Function	Operating Voltage	Stage Placement Criteria (Median)
82A	Q201	Input stage	V_{CE} = 9.2V I_C = 50mA	NF = 1.87 a_o = 0.992
82B	Q202	Intermediate stage	V_{CE} = 10V I_C = 150mA	a_o = 0.0990
82C	Q301	Intermediate stage	V_{CE} = 9.2V I_C = 50mA	C_F = 3.20
82D	Q302	Driver stage	V_{CE} = 10V I_C = 150mA	M_{2E} = −54.2 a_o = 0.986
82E	Q303	Output stage	V_{CE} = 10V I_C = 150mA	M_{3E} = −93.1 a_o = 0.988
82F	Q601	Low band oscillator	V_{CE} = 10V I_C = 10mA	$0.978 < a_o < 0.98$
82G	Q501	High band oscillator	V_{CE} = 10V I_C = 10mA	

uniform in temperature so that low levels of distortion are achieved. This is accomplished by grouping the emitters into four quadrants of nine emitters each, with appropriate spacing between (see Fig. 1). A thermal profile of the 82-type transistor indicates the temperature uniformity across the active element is within a range of 3°C.

2.2.2 Impurity distribution

A unique feature of the transistor manufacture is that each individual silicon wafer of starting material is carefully profiled for the impurity distribution of its epitaxial layer. Poon[1] showed that intermodulation distortion could be reduced by properly shaping the transistor doping profile in the collector region. In practice, optimum low-distortion performance is obtained by grading the epitaxial layer so the concentration of impurity atoms gradually increases in the epitaxial layer in a direction approaching the substrate (see Fig. 2). In processing, the epitaxial profile seen in Fig. 2 is readily achieved by a combination of processing temperature and an appropriately shaped profile at the start. During sub-

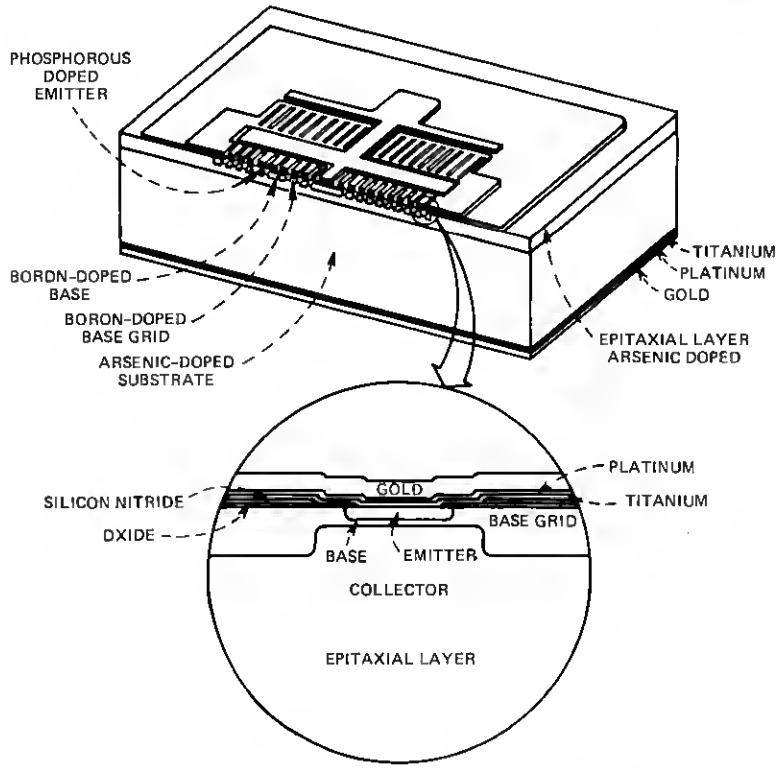

Fig. 1—Cross section of transistor chip. Insert shows enlarged view of a single emitter.

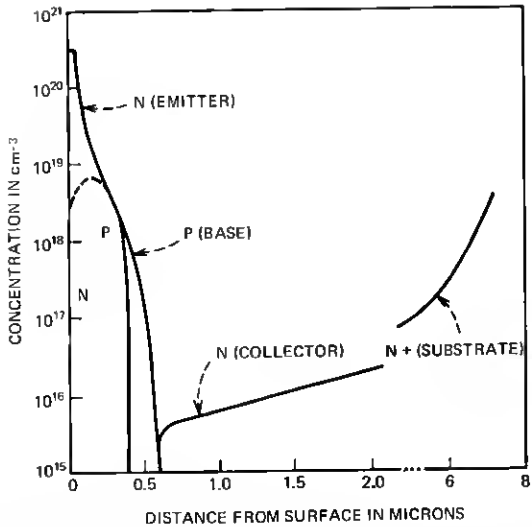

Fig. 2—Transistor impurity profile, with concentration as a function of depth from the surface.

sequent high temperature operations, a redistribution of impurity atoms occurs in just the right amount to produce the desired collector impurity distribution. Intermodulation coefficients represented by M_{3E} below −100 dBm have been realized in this manner. However, early transistor models which were optimized for low distortion by using epitaxial layers 5 μm thick were found to be vulnerable to transient surges. Therefore, to improve transistor surge capability, a 7-μm thickness of the epitaxial layer was found to be necessary. An inherent problem associated with silicon microwave transistors is that the device may go into secondary breakdown in some modes of operation. Use of the thicker epitaxial layer tends to shift the onset of secondary breakdown to higher voltages. This compromise in epitaxial layer thickness resulted in a slight penalty in the third-order modulation coefficient.

Emitter and base impurity distributions shown in Fig. 2 are achieved by straightforward diffusion processes adjusted to meet the transistor's electrical requirements.

Finally, the silicon substrate through which the collector current flows is made thin and is heavily doped with arsenic. Consequently, low collector series resistance, low collector contact resistance, and low thermal resistance are achieved.

2.2.3 Active element

The active element (Fig. 1) consists of 36 emitter stripes. Each emitter is 2.5 μm wide and 65 μm long and is separated by 12.5 μm. The number and size of the emitters were chosen to provide the necessary power

dissipation, low intermodulation distortion, and a flat gain-current characteristic over the operating current range.

A band of deep diffused boron surrounds each emitter and forms a p^+ grid-like structure over the entire active element. This diffusion serves as both a gettering diffusion and as a means of lowering the base resistance between the emitter stripes and at the base contact itself. A combination of a relatively large base contact area and a high surface concentration provides a low base contact resistance (r_b''), necessary for low noise performance. Similarly, a combination of very narrow emitter stripes and stripe spacing and the boron grid provide a low base resistance (r_b'). The active base region is also boron-diffused and is tailored to provide a gain range of $45 < h_{FE} < 160$, an emitter breakdown voltage greater than 5 volts, and a base layer width of 0.23 μm. In summary, the above provides the necessary vertical and horizontal geometry for a gain bandwidth cutoff frequency (f_T) of 2.7 GHz.

The contact metallization used is the Bell System standard titanium, platinum, and gold system. Emitter and base areas are contacted by overlays which lead to wire-bonding pads outside the active element. Collector contact is made through a metallized layer on the back side of the chip.

The titanium-platinum-gold metallization makes use of a new sputter-etch process. This process was first devised by Herb and Labuda[2] and later applied to the transistor manufacture as the first production device sometallized. Even though this appears inconsistent with the policy of using only well-established processes for undersea cable devices, early results were so encouraging it was decided to proceed with the process. In practice, this process is remarkably uniform in quality and manufacturing yields when compared to the older plating process.

Briefly, the process consists of depositing uniform layers of Ti, Pt, and Au; masking the contact areas with nickel plate; and then rf sputter-etching away those areas not wanted. The mechanism depends on the relative etch rates of the various materials used.

2.2.4 Device stabilization

Traces of metallic impurities are always present in semiconductor starting materials and sometimes are introduced in subsequent processing steps. They are known to degrade electrical properties of semiconductor junctions and upon their removal the junction characteristics are restored. Any scheme which removes or immobilizes these impurities is considered a gettering process.

Two such processes are successfully used in the transistor processing. The first makes use of a high concentration, deep, and highly stressed diffusion region in the transistor's active element. As mentioned earlier, a deep boron-diffused grid-like structure is formed in the base area to

create a p^+ region in the proximity of each emitter stripe. A diffusion such as this is known to have two important properties: (*i*) the enhanced solubility of metallic impurities in a p type diffusion, and (*ii*) the high density of dislocations associated with this type of boron diffusion.[3] Both these effects, as well as their close proximity to the emitters, result in a very effective gettering mechanism. Junction leakage currents have been reduced several orders of magnitude to a few hundredths of a nanoampere. Furthermore, the transistor exhibits a very flat gain-current characteristic at low currents (Fig. 3) which can be attributed to the reduction in the number of recombination sites in the gettered base region.

The second gettering process is used on both transistors and diodes, which contain silicon dioxide and nitride layers. Because stability of surfaces is so important in establishing reliable device operation, these layers are, in addition to other functions, used where appropriate in passivation techniques for controlling semiconductor surface potentials. However, silicon dioxide is known to be porous to alkali metals, particularly sodium ions. These ions can migrate to the silicon surface and alter the electrical characteristics of the device. Every effort possible is exerted in manufacture to eliminate these contaminants but, as a precautionary step, the device is protected by a silicon nitride coat which is placed over the oxide as a permanent seal. In addition, immediately before the nitride coat is applied, the underlying layers of oxides are given a gettering treatment to rid them of possible ionic contamination.

The final step in device stabilization is a high temperature anneal of each completed transistor wafer to relieve any stresses introduced during the metallization operations.

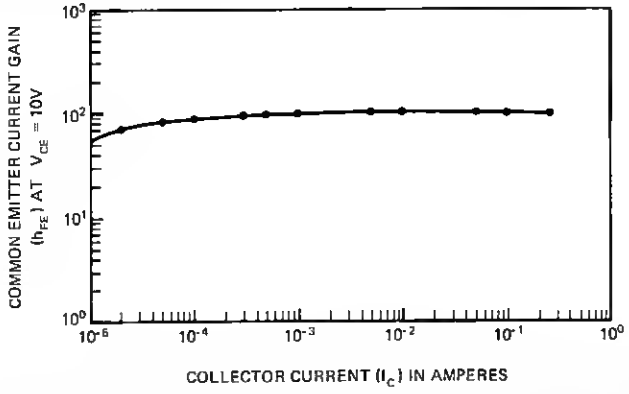

Fig. 3—Common emitter current gain characteristics, with transistor gain as a function of collector current.

2.2.5 Encapsulation

Because operating temperature is so important a factor in establishing device reliability and performance, a significant amount of effort is invested in the design of low thermal impedance packages. Furthermore, these packages are required to remain vacuum tight over substantial excursions of temperature and time. They must consist of materials that do not introduce excessive stress on the fragile semiconductor chip.

The structure chosen for the transistors and diodes is a hermetically sealed encapsulation which provides alumina ceramic isolation for low parasitic capacitance and inductance, stud mounting, and low thermal resistance. The transistor combination of the active element and package has a thermal derating factor of less than 24°C per watt. This is consistent with the thermal objectives of the system, whose goals are based on a maximum operating junction temperature of 65°C. Although the package was developed specifically for the transistor, it is also used for diodes to simplify manufacture.

The encapsulation features are also based on providing the transistor or diode with the best possible environment during its lifetime, even with the device active element itself equipped with a passivated design. Charge accumulation is enhanced by the presence of water vapor and electrolysis contributes to degradation of internal structural members; therefore, all semiconductor devices are hermetically sealed. Also high temperature baking of piece parts and cold-weld closures minimize the chance of residual gas evolution inside the enclosure after the seal is made.

Figure 4 is an illustration of the package. This encapsulation consists of two subassemblies (a header assembly and a stud can assembly). These assemblies are joined together by a cold-welding process after the semiconductor chip is bonded to the header and the connections to the feed-through leads have been made.

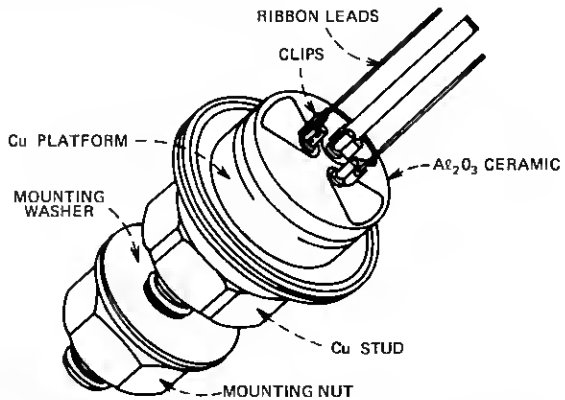

Fig. 4—Semiconductor device encapsulation. Diodes and transistors are hermetically sealed in this package.

The header assembly consists of a number of separate piece parts brazed together. The welding flange of the header assembly is fabricated from oxygen-free high-conductivity copper using cold forming operations. The molybdenum platform, upon which the semiconductor chip is mounted, is punched from special material which will not delaminate during fabrication. Ceramic insulators consist of an aluminum oxide disc metallized with a mixture of molybdenum and manganese, over which a thin layer of copper is plated. Feed-through terminals are made of Kovar lead wire and Kovar washers. All parts are brazed together simultaneously using special brazing alloys, and the final assembly is then finished with layers of nickel and gold plate.

Can assemblies are also made of separate piece parts. The stud is cold formed of an alloy of copper selected to meet the torque requirements necessary to ensure good thermal contact to the repeater housing. The can is formed from oxygen-free copper and is ultrasonically welded to the stud. The assembly is finished with a nickel and a gold plate.

To ensure reliability and integrity for the package, a number of tests and examinations are performed during assembly and upon the completed package. Some are destructive sampling tests and designed to determine failure limits. An example is hydrostatic pressure testing until rupture occurs. Another test is a lead push test, in which force is applied axially to the end of the lead of the header until it is pushed through the ceramic.

As part of the final screening of devices, the package is again scrutinized for mechanical defects by exposing the devices to acceleration tests, shock tests, and particle tests as well as detailed visual examination.

2.3 Characterization

Electrical characterization of underseas cable semiconductor devices is, of necessity, a detailed and exacting process. The high system performance objectives and the rigorous reliability goals require testing procedures not usually applied to ordinary devices. For example, the reliability objectives for the transistor demand that a change in common emitter current gain (h_{FE}) be no more than 2.5 percent over the service life of the transistor. This is equivalent to a change in small signal current gain (a_o) of less than 0.0005 over a 20-year period. Therefore, these devices must not only be designed to meet such stability requirements, but must be characterized to such a degree that it can be determined that such minute changes can be detected. Toward this end a battery of tests is performed, some of which are repeated many times during the screening program.

Characterization is in two parts: dc tests primarily determine the reliability qualities of the device, RF tests show mostly the circuit perfor-

mance capabilities. In addition to conventional dc tests, several of which are performed at multiple bias points, special tests such as pulse tests and surge capability tests are conducted. Transistor current gain measurements are made at several levels of collector current on each individual device.

Two tests are made at use conditions (50 and 150 mA), one test is made at a level very sensitive to transistor changes (5 mA) to monitor aging and selection, and another is made at high current (250 mA), which is a good indicator of whether all emitters are properly functioning. Each candidate transistor must be able to meet the gain-current characteristic shown in Fig. 3.

Another example of special testing is the test placed on the transistor's emitter junction. The quality of the emitter junction is particularly critical because of its exposure in service to noise overload which may momentarily push the emitter into reverse conduction, its exposure to residual surges which act similarly on the device and stem from cable fault, and its exposure to inverse bias which may occur temporarily during fault monitoring. Therefore, the shape of the emitter reverse voltage-current characteristic is critical and must be determined for each device. Table II shows typical dc characteristics of the transistor.

RF testing consists of four noise figure measurements, ten intermodulation coefficient measurements, and "on-line" transistor modeling of each device. On-line modeling is transmission characterization performed on a computer-operated test system which produces a circuit model for each transistor. The S parameters of each transistor are measured at the two use conditions and at 15 frequencies from 0.1 MHz to 436.8 MHz. These data are automatically fed into a computer and by means of a circuit-oriented model (Fig. 5) reduced to six basic parameters. The model is constructed so that it fixes the values of those transistor elements which are not likely to vary widely in manufacture. Fixed values shown in Fig. 5 are calculated from the geometry, impurity concentration, etc., for a typical transistor. The variable elements are (*i*) small signal current gain a_o, (*ii*) capacitance associated with a_o cut-off frequency *Cep*, (*iii*) collector/base capacitance less inner capacitance C_F, (*iv*) total emitter resistance R_e, (*v*) total emitter inductance, L_E, and

Table II — Some typical DC characteristics

I_{EBO} (V_{EB} = 2V)	<0.35nA
I_{EBO} (V_{EB} = 3V)	<10nA
I_{EBO} (V_{EB} = 4V)	<235nA
I_{CBO} (V_{CB} = 10V)	<0.07nA
I_{CEO} (V_{CE} = 10V)	<0.09nA
BV_{CBO} (I_C = 100 μA)	>60V
BV_{EBO} (I_E = 100 μA)	>5V
V_{CB}, V_{EB} (I_E = −100mA)	<0.91V
h_{FE} (I_C = 150mA, V_{CE} = 10V)	$50 < h_{FE} < 160$

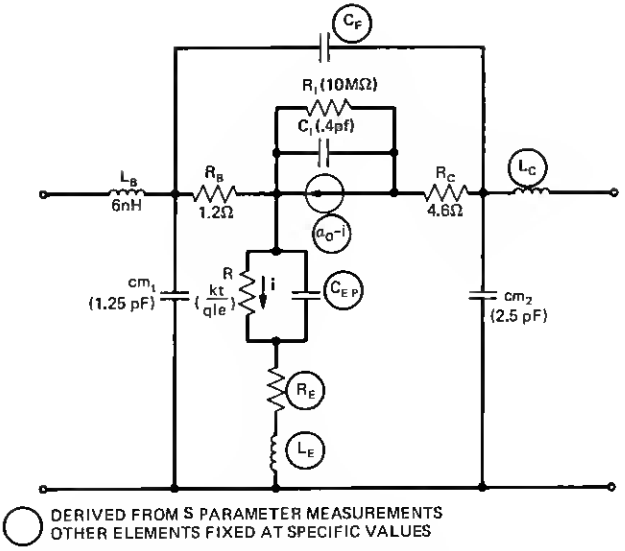

Fig. 5—Circuit-oriented model used to establish transistors' behavior in a repeater set. Circled elements are varied to match data. Other elements are calculated from geometry and impurity distribution.

(*vi*) total collector inductance L_c. Distributions of all RF parameters are compiled, and each transistor is assessed with respect to its relative position in the total population. It is then assigned to a specific repeater set where it has a unique and optimized function. Table III illustrates how tightly the model parameters are controlled for TAT-6.

2.4 Screening and aging

Although, in essence, mechanical screening begins at the very onset of manufacture, a series of mechanical evaluations is performed on all completed devices to confirm the integrity of the device's structure. Electrical screening begins with environmental stresses such as channel aging, overstress power aging, and high temperature stress, and ends with long-term aging.

Channel aging is done on a 100-percent basis and serves to eliminate inferior devices that, despite all the precautions taken in manufacture, may still have some surface charge accumulation. This is accomplished by holding each device at elevated temperature with its junction at reverse bias for a period of one week.

Accelerated power aging is a shakedown test. Each transistor is power-overstressed at a level three times its operating level (4.5 W) for a period of one week. This test is well within the capability of the transistor structure and enables detection of devices with marginal quality and incipient failure modes.

Table III — 82 type transistor—AC model parameter data

	82A*		82B†	
	-2σ	$+2\sigma$	-2σ	$+2\sigma$
a_o	0.9894	0.9932	0.9842	0.9926
$R_e(\Omega)$	0.1530	0.1962	0.1729	0.2156
C_F(pF)	3.035	3.863	3.011	3.679
C_{EP}(pF)	111.2	151.3	292.3	462.0
L_E(nH)	6.535	6.833	6.565	6.891
L_C(nH)	6.024	6.689	6.314	6.892
	82C*		82D†	
	-2σ	$+2\sigma$	-2σ	$+2\sigma$
a_o	0.9818	0.9926	0.9808	0.9900
$R_e(\Omega)$	0.1455	0.1956	0.1712	0.2176
C_F(pF)	3.131	3.452	3.015	3.529
C_{EP}(pF)	120.2	202.3	340.3	486.6
L_E(nH)	6.543	6.868	6.554	6.892
L_C(nH)	6.010	6.674	6.348	6.848
		82E†		
		-2σ		$+2\sigma$
a_o		0.9814		0.9925
$R_e(\Omega)$		0.1669		0.2155
C_F(pF)		3.085		3.745
C_{EP}(pF)		317.8		466.4
L_E(nH)		6.566		6.889
L_C(nH)		6.318		6.814

* (V_{CE} = 9.2V, I_C = 50 mA).
† (V_{CE} = 10V, I_C = 150mA).

The high-temperature stress technique is a sampling test based on the observation that semiconductor device life is related to the magnitude of the stressing temperatures. A sample of every lot of transistors is stressed at three different time intervals and three junction temperatures. Distributions of failure based on the reliability goals (Δh_{FE} < 2.5% in 20 years) are then made for each time and temperature combination. From these data, the commonly known Arrhenius Failure Distribution (Fig. 6) is made which provides a convenient method of determining the failure rate for any time-temperature combination. Inspection of these acceleration life curves reveals that the sigma of the failure distribution remains constant at various stress levels; therefore, we may extrapolate the curves in Fig. 6 to long-time, low-stress-level conditions. Note in Fig. 6 that the intersection of the 20-year objective with a 65°C use condition (these being the reliability objectives) is coincident with a value of sigma of tbe transistor failure distribution, which is extremely small. This establishes the confidence level or percentage of failure to be expected. With six transistors in each repeater of the 700-repeater system, these extrapolations indicate that in 20 years one would anticipate less than one transistor failure in the entire system.

Finally, the devices are placed on six-month long-term age at maxi-

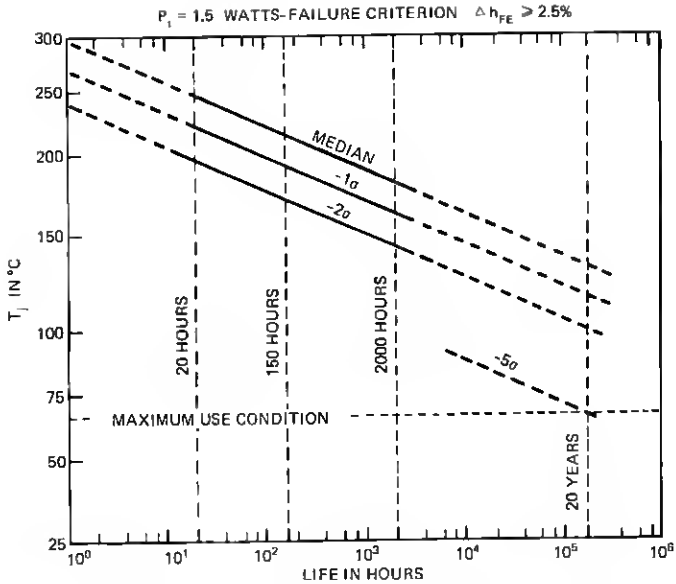

Fig. 6—Pattern of accelerated aging for transistors.

mum operating conditions. During this time, devices are tested at regular intervals, the results of which are observed for trends. These data are statistically extrapolated over a 20-year period, with the objective of assuring a 20-year life in the repeater. Figure 7 is a graph of how a group of SG transistors age. The graph contains a plot of the median as well as the standard deviation in the population. After initial stabilization, no further trends are evident.

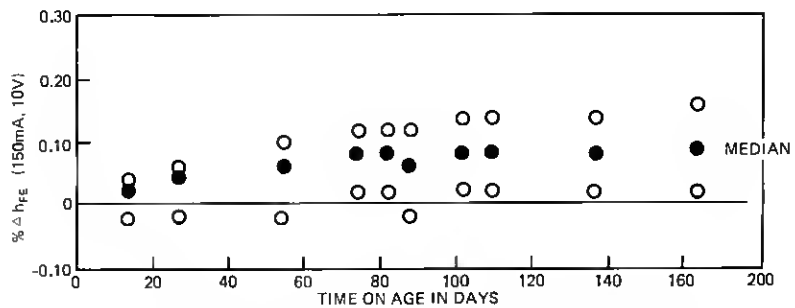

Fig. 7—Stability of a group of transistors during long-term aging.

2.5 Transistor improvements for future systems

Upon completion of transistor manufacture for TAT-6, several important design improvements were made to the 82-type transistor. The transistor's surge capability was significantly upgraded by fabricating the device in double epitaxial silicon, where the normally lightly doped thin epitaxial layer is separated from the heavily doped substrate by a thick epitaxial layer of intermediate doping level. Use of the double epitaxial layers shifts the onset of secondary breakdown to higher power levels while still maintaining good linearity and high frequency performance. A compromise in epitaxial thickness as reported in Section 2.2.2 is no longer necessary. Furthermore, unexpected high distortion near the upper end of the transmission band was markedly reduced by changing the orientation of the starting silicon material from ⟨111⟩ to ⟨100⟩. Experimental devices indicated interface surface effects were the cause of this anomalous behavior. Moreover, a recent study by Olson[8] shows surface effects can contribute to intermodulation distortion.

Another important change concerns the semiconductor device encapsulation. Gold-plated piece parts that make up the package have been replaced by unplated nickel parts at a considerable cost savings with no penalties in reliability or integrity of the encapsulation. And finally, additional high-temperature annealing of the assembled transistors prior to final sealing has further enhanced the transistor's stability. The slight change in gain during the initial period of aging under operational conditions (Fig. 7) is no longer evident, so that now the transistor is essentially stable from the very beginning.

III. DIODES

3.1 Requirements

A total of seven diode codes are used to obtain the required protection for each repeater. They consist of three basic types, two of which are similar to those used in the SF system.

The 522 is a silicon planar diode used for signal overload protection and is new for the SG system.

The 523B,C,D,E, and F are silicon mesa-type diodes. Specifically, the 523B acts as an amplitude control for the oscillator, the 523C furnishes input protection for the preamplifier, and the 523E is used for signal path surge protection and is located in the directional filter.

The 524A is also a silicon mesa-type diode and is used as a voltage limiter for power path surge protection in the ground separation filter. They are used in a set of three in parallel, packaged as the 532A. In the event of a cable break or large transient through the repeater, these diodes must regulate the peak voltage across the repeater during the transient. Table IV shows the diode complement.

Table IV—Location and characteristics of diodes

Diode Code	Circuit Designation	Function	Operating Voltage	Critical Characteristic
522A	CR-301	Output transistor signal overload protector	−0.8V	C < 10 pf series resistance 10 to 13 Ω
523B	CR-501	High/low band oscillator amplitude limiters	0V	max. C/pkg. = 20 pf
523C	CR-201	Signal path surge protectors	−0.85 (each chip)	max. C/pkg. = 8 pf chip Δ = <1 pf
523D	CR-401	Signal path surge protectors	−12V	max. C/pkg. = 4.8 to 5.8 pf
523E	CR-101	Signal path surge protectors	−4V (each chip)	max. C/pkg. = 11.6 to 12.6 pf
523F	CR-402	Signal path surge protectors	−12V (one chip)	max. C = 4.8 to 5.8 pf
532A	CR-701	Power path surge protector	−12V	forward characteristic matched to within 0.1V @ 75A/set of 3 V_{BR} = 15V @ 10mA

3.2 Design

New for the SG system, the 522A employs a planar technology similar to that of the transistor, including silicon nitride passivation. The design is tailored to provide protection during signal overload to the emitter-base junction of the output transistor of the power amplifier. Signal overload can result in reversing the bias of the emitter-base junction, causing it to go into breakdown. This is known to degrade stability characteristics of the transistor. Diode characteristics which will provide this protection during signal overload and which would not alter the current during normal signal levels are seen in Fig. 8.

To meet these requirements, a small gold-doped silicon chip was designed. Small area keeps the capacitance low, and gold doping controls the slope of the forward V-I curve after forward conduction begins. The diode junction is formed by boron diffusion and protected by a silicon nitride layer. To achieve the required forward V-I characteristic, a thin layer of gold is evaporated on the back of the wafer and diffused into the silicon. This lowers the lifetime of the minority carriers and increases the series resistance of the diode. Contact metallization is provided to the chip by a nickel-gold overlay.

The chips for the 523 and 524 diode types are similar in design to 468A and 467A used in the SF system[4] and include a silicon dioxide passivation layer over the junction area.

The 522A chip is mounted in the same SG package as the transistor. The 523 type chips are also in the same package but are mounted in series, two to a package. The 524A is mounted in a slightly modified one-lead version of tbe basic SG package and then mounted on a heat sink as a matched group of three diodes (Fig. 9).

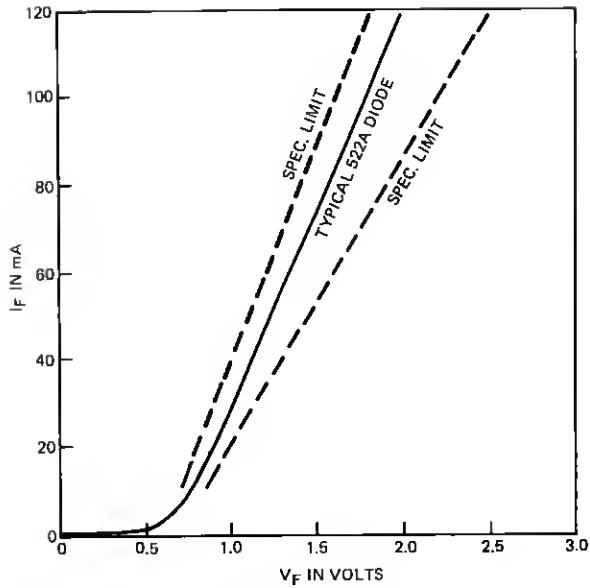

Fig. 8—Forward characteristics of a 522A diode.

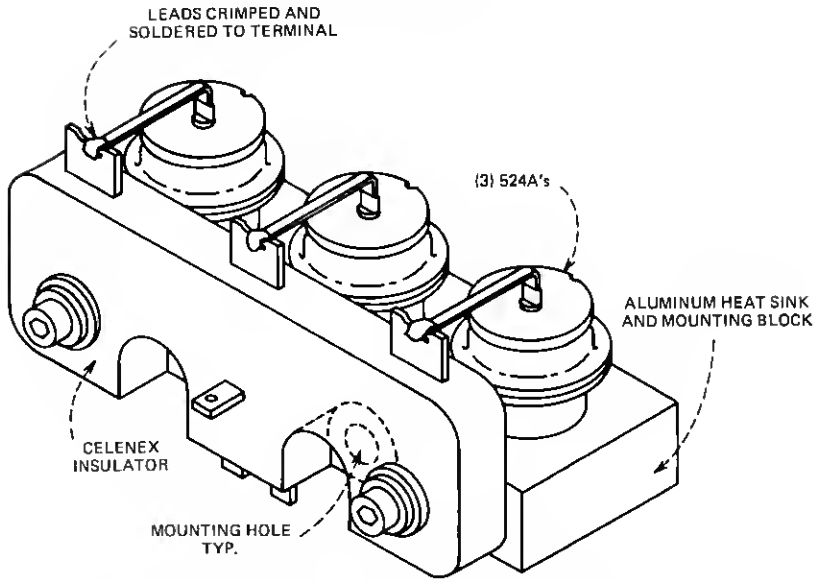

Fig. 9—Matched diodes mounted on a heat sink and connected in parallel.

3.3 Characterization

A battery of tests is performed, some of which are repeated many times during the course of the screening program. In addition to the normal diode tests of saturation current, forward and reverse voltages, surge

tests, etc., specific tests are performed on the various codes. For instance, the diode characteristic curve in Fig. 8 is ensured for each 522A by measuring the forward voltages and currents at a number of operating levels. The 523 family of diodes which contains two chips is characterized for each chip and the combination of the two chips, and then fitted to the specific protective functions (see Table IV).

Finally, the 524A which is the basic building block for the 532A surge protector is characterized by measuring the individual diode breakdown voltages during a 75A surge and then matching them to within 0.1 V for the three diodes set.

3.4 Screening and aging

Screening consists of channel age tests, accelerated age, and operational aging at use conditions. The channel age test consists of holding the diode at reverse bias for 16 hours at 150°C and at 80 percent of the breakdown voltage. The accelerated age test consists of holding the diodes at high temperature for 144 hours. Devices that behave differently from the main populations are discarded, and the remaining diodes are aged for six months at maximum use conditions. Those diodes that exhibit the most stable characteristics are then selected for use in the repeater.

The aging characteristics of SG diodes are similar to those of the SF system, in which many years of accumulated data indicate unprecedented reliability.[5]

3.5 Device manufacture

The manufacture of semiconductor components makes use of the principles devised for the devices used in earlier undersea cable systems. To reduce the possibility of unforeseen sources of device instability, all manufacturing operations are meticulously performed under stringent conditions. All the crucial operations are performed in a clean room environment. Raw materials and piece parts are inspected to assure conformance to the design intent. Thorough records of all inspections are kept, to create an atmosphere of quality consciousness and to provide diagnostic information in the event of deviant behavior of devices or device lots. Control charts are used to monitor the uniformity of the processes, and inspections take place at every step in the manufacture to prevent introduction of incipient failures. Pedigree data on each device is stored so that any particular device is traceable from its material point of origin throughout its history in the manufacturing shop.

In the SG program, many new and sophisticated pieces of apparatus were used to improve precision and control. Furnace operations such as oxidation, diffusion, and annealing are all performed in an automatically controlled furnace complex. This system achieves with fine pre-

cision the processing repeatability and uniformity required for device manufacture. Process variables such as gas flow, temperature, insertion and withdrawal times, speed, and other related parameters no longer involve human variability. Vacuum deposition stations used in metallization operations are similarly automated. Wafer separation is accomplished by laser-beam cutting. Finally, a specially constructed, scanning electron-beam microscope is used to inspect each individual device before it is sealed in its encapsulation.

IV. GAS TUBES

Primary signal path surge protection is accomplished by four WE 469A gas tubes similar to those used in early undersea cable systems.[6]

V. RESISTORS

5.1 Choice

Tantalum nitride film resistors were chosen for the SG system because of their stability, the predictability of their aging characteristics, and their low parasitic effects. In addition, their performance in the Bell System as well as in the SF undersea cable system[7] has been excellent.

5.2 Requirements

Resistors are used in bias networks, current limiting, feedback networks, wave shaping, equalizers, impedance matching, and level adjustment. Tolerances range from ±15 percent for some of the low-valued resistors to ±0.1 percent for others in critical applications.

Two sizes of resistors are required. Type 265 resistors are rated at $\frac{1}{8}$ W but are operated at a maximum of $\frac{1}{16}$ W, at which power the film temperature is such as to guarantee end-of-life tolerances well below those required by the system. Type 266 resistors are used in the repeater output stage and are rated at $\frac{1}{2}$ W but are operated at a maximum of 0.3 W to keep end-of-life tolerances well within system requirements. There are fifty-nine 265-type resistors and fifteen 266-type resistors in the repeater. A typical ocean-block equalizer may contain one hundred nine 265-type resistors, of which twenty-two are used for "mopping up." Resistor patterns range from 0.6 square to 250 squares. Although the SF system used resistors formed on sapphire (the 243-type), considerable experience since has demonstrated that resistor films on bare alumina substrates possess more than sufficient stability for the SG application. In addition, the use of alumina substrates amounts to a considerable cost saving.

5.3 Construction

Resistors range in value from 3 to 10,000 ohms and are fabricated using as-sputtered sheet resistances ranging from 4.5 to 25 ohms/square.

Both 265- and 266-type resistors are made by sputtering the appropriate tantalum nitride film onto 9.52 × 11.43 cm (3¾″ × 4½″) ceramic substrates, followed by evaporated layers of titanium and palladium, over which is plated 3 μm of gold. Resistors are patterned photolithographically and are laser-scribed into "mini" substrates 2.54 cm (1 inch) square. These squares contain ten 265- or four 266-type resistors which are then pre-anodized, heat-treated, and then final-anodized to value. Then the squares are sawed apart into discrete resistors, and leads are attached by thermal compression bonding. A pre-stamped polyvinylidene fluoride sleeve is shrunk over the resistor for protection. The stamped information on the sleeve includes the sputter run number, the substrate number in the run, the "mini" number, and the individual resistor number from the "mini," thus allowing complete traceability for each individual resistor. Complete resistors are shown in Fig. 10.

The resistors are assembled by gold-to-gold thermocompression bonding, thus precluding whiskers and other possible intermetallics.

5.4 Screening and reliability

The resistors are heat-treated in "mini" form for two weeks at 150°C to determine resistor film quality. Then assembly of the resistors is

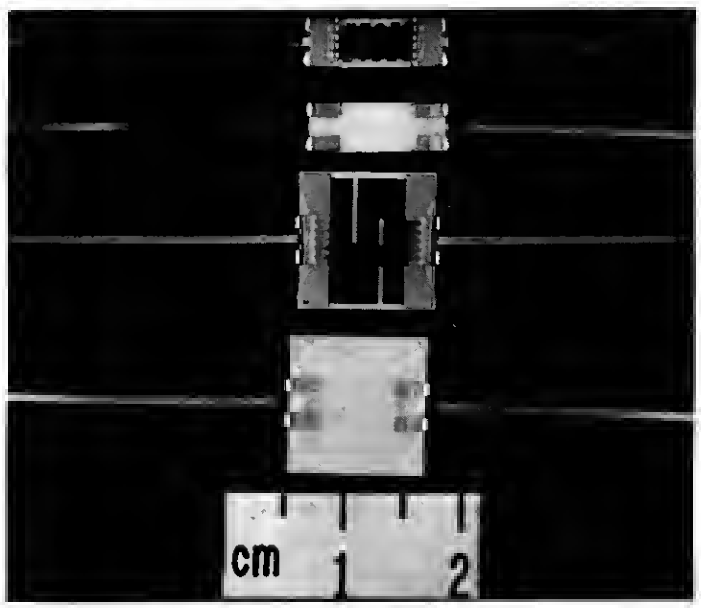

Fig. 10—Thin film resistors.

completed, and they are shipped to the repeater assembly location where each resistor is visually examined, a sample of the product is voltage-surge tested, then all resistors are baked 24 hours at 105°C, followed by five temperature cycles from −40° to +85°C. After that, each resistor sustains a short-time overload of 6.25 times rated power for 5 minutes. This is followed by 1,500 hours at rated power to screen out any resistors with anomalous behavior and, after a final resistance check and noise measurement, the resistors are ready for assembly. Overall yield after screening and testing is 75 percent.

VI. CAPACITORS

6.1 High-voltage paper capacitors

As described elsewhere in this publication, the coaxial cable supplies dc power at constant current to operate each repeater, as well as carrying the composite carrier signals being transmitted in both directions. To separate the dc power from the carrier signals, power separation filters are included on each side of the repeater amplifiers (see Fig. 11). Sufficient dc power is tapped off to power the repeater, and the dc current is returned to the cable. The major source of destructive high frequency feedback around the repeater results from the series inductance in the path between the "sea" ground and the internal repeater ground. It is possible to eliminate this inductance by making the signal path a completely coaxial structure in which the outer conductor comprising a coaxial capacitor is used to "connect" the two grounds (see Fig. 11).

6.1.1 Choice of capacitor materials

The coaxial capacitor must be able to stand the full cable voltage (7 kV) plus any anomalous spikes generated during fault conditions. Consequently, castor-oil impregnated kraft paper capacitors were chosen for this service, as they have been for earlier submarine cable systems, with excellent results.

6.1.2 Requirements

The maximum voltage sustained by these capacitors at the shore ends of the system is 7 kV. Capacitance value is 13 nF ±3 percent. The smallest physical size together with the required coaxial structure and voltage rating dictated the unit shown in Fig. 12. Notice the tube with expansion bellows to allow for the expansion of the castor-oil-impregnant, particularly during the high-temperature processing which the repeater undergoes. Coaxial construction plus near-perfect axial electrical symmetry reduces series inductance to 20 nH.

6.1.3 Construction

As can be seen in Fig. 13, this capacitor is actually two capacitors in

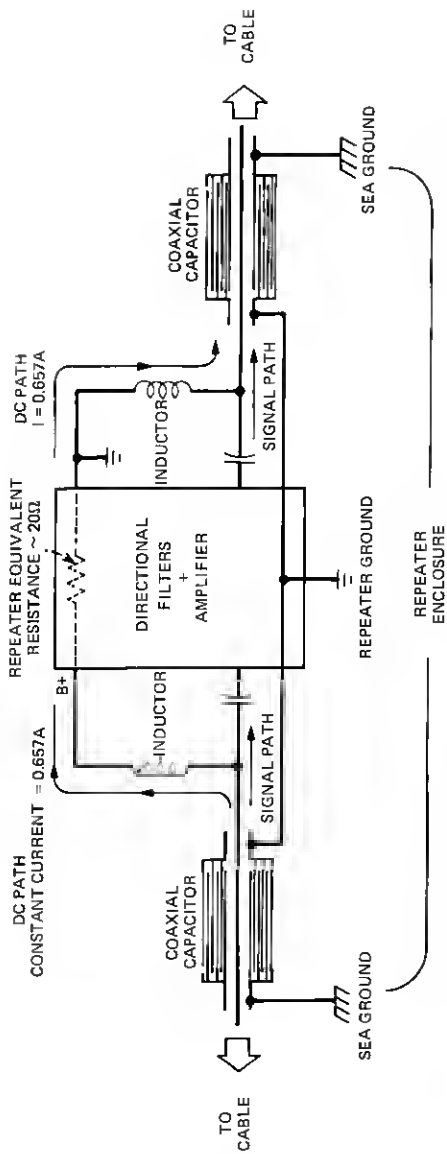

Fig. 11—Diagram showing how coaxial capacitors are used to "connect" the "sea" ground and the repeater ground.

Fig. 12—Completed coaxial capacitor used in ground separation filter. Note expansion bellows.

series. Notice how the conducting foils are interleaved so that there is a "floating" foil not attached to the external connections. The capacitor is wound on a hollow alumina ceramic tube with metal ferrules soldered to it at both ends. The floating foil plus the connected foils are separated by 5 layers of 25-μm (1-mil) paper. Foils are approximately 6-μm ($\frac{1}{4}$-mil) thick aluminum. This combination of papers and foils is wound to the appropriate diameter (and capacitance value) with conductor "flags" attached to the outside foils at positions that are axially symmetrical and 90 degrees apart around each end of the capacitor. This symmetry is necessary to keep the series inductance of the structure as low as possible. The capacitor is completed by enclosing the paper-foil unit in a ceramic housing which is soldered in place. One ferrule is equipped with the expansion bellows plus a filling tube where the oil enters the unit. After a vacuum bake, the capacitor is impregnated with pure castor oil and sealed. All external metal parts are nickel + gold plated for solderability and to eliminate corrosion. Nickel is included as a diffusion barrier.

Other high-voltage capacitors used in the equalizers are constructed in a similar manner, but are not in a coaxial configuration.

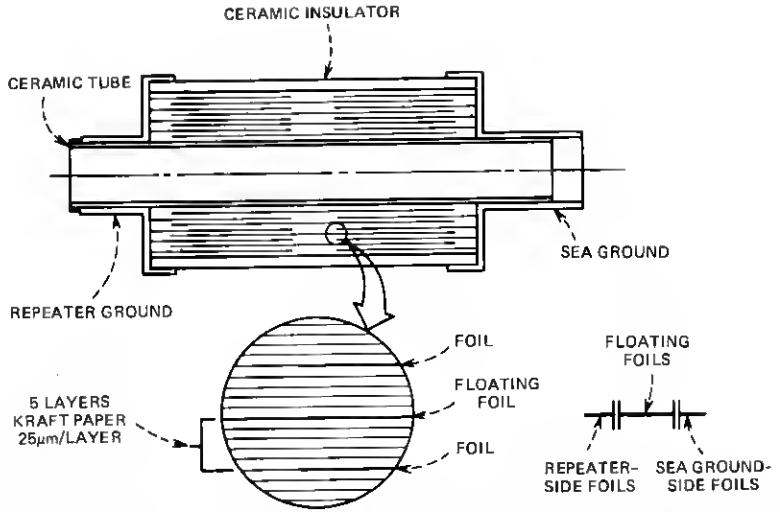

Fig. 13—Diagram showing cross section of coaxial capacitor (expansion bellows not shown).

6.1.4 Qualification and testing

Every roll of capacitor paper purchased is qualified for use by testing capacitors made from the paper. These test capacitors are wound and impregnated with castor oil, tested for 25 days at 66°C and more than twice-rated voltage. Capacitance and insulation resistance shifts are checked as well as catastrophic failure.

Ten percent of all manufactured product is sacrificed for a similar test, and all product is screened for 6 months at sea-bottom temperature (4°C) and at higher than rated voltage. During these tests, all significant electrical parameters must remain within tight limits.

Capacitance tolerance for this application is ±3 percent, with a total shift during life of perhaps 0.5 percent. Capacitors are initially stabilized by temperature cycling between −18°C and +66°C, and capacitance shifts are again held to tight limits. Insulation resistance and effective series resistance at 100 kHz (a measure of internal, stable, electrical continuity) are both held to absolute values; the change in those parameters during processing and aging is also held to tight limits.

6.2 Ceramic capacitors

6.2.1 Choice

Previous submarine cable systems used mica capacitors because of their excellent trouble-free history of providing stable, reliable operation at sea-bottom temperatures. The parasitic performance of mica capacitors at SG frequencies, however, precludes their use. Ceramic capacitors were chosen instead, although their long-term reliability had to be es-

tablished as part of the program. Results of testing and screening to date have shown this choice to have been a good one.

6.2.2 Requirements

As Western Electric does not manufacture ceramic capacitors, the required units are purchased from outside suppliers under specification KS-21013. Required values range from 3 pF to 0.047 μF, with 80 percent of the values less than 1000 pF. Tolerances range from ± 5 percent to ± 0.2 percent, with the majority of applications requiring ± 1 percent. Ceramic capacitors are available in a range of temperature coefficients but, for this application, NPO (zero temperature coefficient) capacitors are used because their capacitance stability with temperature averages better than ± 0.02 percent. There are no applications where the less temperature stable, high-K dielectric capacitors would suffice, in spite of their smaller size.

6.2.3 Construction

Ceramic capacitors use a thin (37 μm), modified titanium dioxide ceramic as a foundation onto which are screen-printed palladium electrodes. The ceramic sheets are piled up and punched into stacks which are pressed and fired. The resulting "chip" with alternating electrodes emerging from each end is coated on the ends with a fritted silver, which is then fired, thus connecting alternating electrodes together (see the cross section in Fig. 14). The completed chip is measured for capacitance and other parameters and then sorted into a "post office" of graded values, which are then paired to give the correct total value. Leads are soldered to the paired chip which is then mounted into a molded diallyl phthalate case and encapsulated with a silicone rubber potting material (see Fig. 15). After testing, capacitors are finally mounted into the appropriate printed wiring board.

The copper wire leads are nickel- and gold-plated to keep them cor-

Fig. 14—Cross section of ceramic capacitor.

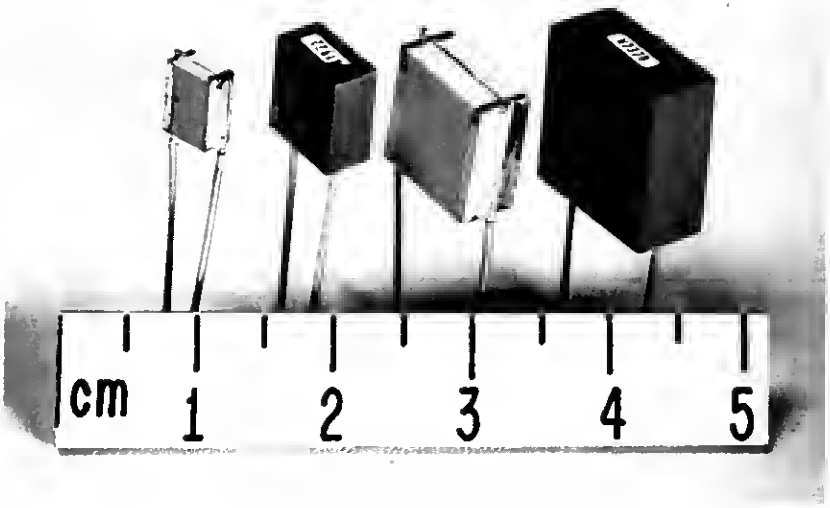

Fig. 15—Ceramic capacitors.

rosion-free and solderable. The nickel is used as a diffusion barrier between the copper and gold.

6.2.4 Screening procedures

With the application of voltage, ceramic dielectric undergoes an electrochemical degradation which eventually results in breakdown. The preliminary accelerated life testing of 3500 capacitors of the type to be used under a variety of conditions led to the conclusion that under sea-bottom conditions their average life would be over 100,000 years, but that it would be necessary to screen out atypical capacitors that might fail much earlier.

All capacitors undergo a rigorous testing program by the supplier, and a sample of each lot is subjected to destructive electrical and mechanical tests to determine the capability of the lot.

After delivery to Western, the capacitors are subjected to additional testing. To screen out any which may have an intermittent internal connection, each capacitor is cycled over the entire operating and storage temperature range (−20° to 60°C) twice while it is continuously monitored for capacitance. The capacitors are also life-tested at voltages ranging, according to dielectric thickness, from 150 to 450 V dc. Electrical parameters are monitored and compared before test, after two months of test, and after four months of test. Both fixed and statistical limits are placed on the values and the changes in value, to screen out any units which could be peculiar.

6.2.5 Reliability

In 96,702 capacitors screened, 8 short-circuited on the four-month life test. Assuming that the failure rate is proportional to the third power of the applied voltage, they would short-circuit at the rate of 0.005 FIT* in the system.

6.3 Solid tantalum capacitors

6.3.1 Introduction

Solid tantalum capacitors were used extensively for the first time in the SF submarine cable system. They are particularly useful because of their large capacitance density. Twenty solid tantalum capacitors are in each SG repeater: fifteen 1-μF and five 10-μF units (see Fig. 16). They are used exclusively as coupling and bypass elements, since their characteristics do not allow their use as elements in frequency-sensitive networks.

6.3.2 Screening procedures

All capacitors are measured for capacitance value, series resistance, and leakage current as they enter the Western Electric, Clark, New Jersey shop. Then, at specified periods during nine months of screening, they are measured for the same parameters four more times. Screening

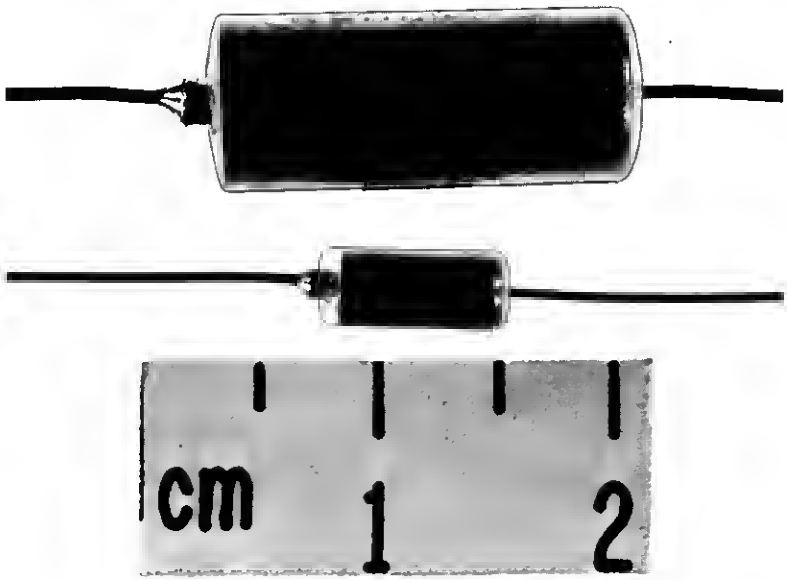

Fig. 16—Tantalum capacitors.

* Number of failures in 10^9 hours.

consists of temperature cycling, pulsing, surge testing, and life testing for three 60-day periods at elevated temperature and voltage.

After these tests, any unit displaying a ±0.5-percent change in capacitance is rejected. The absolute differences in successive readings of series resistance and leakage current are limited to fixed maximum values. In addition, the results are looked at statistically, so that any units showing absolute differences outside 3.5σ for either parameter are rejected.

VII. INDUCTORS AND TRANSFORMERS

7.1 Transformers

Transformer designs for undersea cable systems are influenced profoundly by the ratio of highest-to-lowest transmitted frequency. The SB, SD, and SF systems all maintained a ratio of about 12:1. In the SG system, however, this ratio has been increased to 50:1. The 30-MHz top frequency requires smaller designs to reduce parasitics, but sizes should not be so small that the low-frequency characteristics are degraded or the reliability is compromised.

Figure 17 shows the signal transformer designs. The 2678B/C is used either as an input or output transformer, while the 2678A is used for interstage coupling. All are "transmission line" transformers, and the input and output units are designed as hybrids. All use the same toroidal

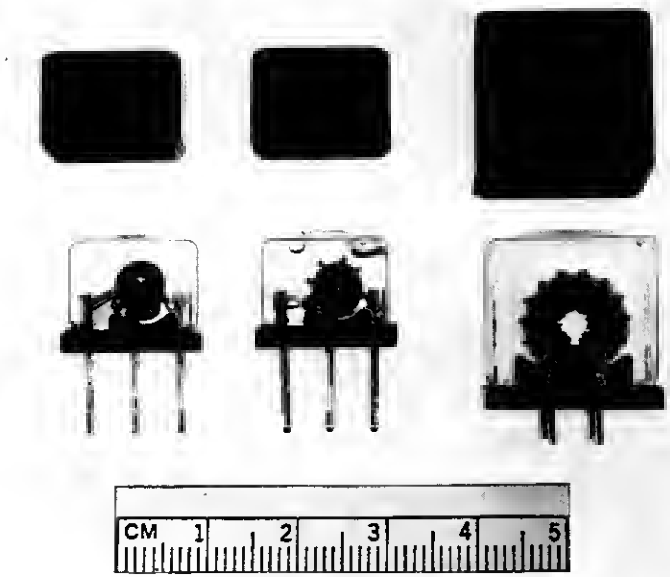

Fig. 17—Signal transformers.

core material, a newly developed manganese-zinc ferrite. The electrical integrity of these units must exist well outside the system's bandwidth, where overall gain and phase of the feedback amplifier continue to be important.

The 2679A transformers are used in such a way that their parasitic capacitance and short-circuit inductance become elements in the directional filter. Consequently, this puts a premium on the reproducibility and stability of these components. This is achieved by making the winding from a pair of wires, twisted under controlled tension at a specified number of turns per inch.

Figure 18 shows the 2680A longitudinal choke whose purpose is to suppress longitudinal currents while remaining transparent to the transverse signal voltages with no more than a 2-percent reflection coefficient. Its self-inductance is part of the power separation network; as such, it must carry the 0.657-A cable current. It is designed to withstand the 8-kV surge which could appear between the windings in the event of an accidental cable cut near shore. This combination of re-

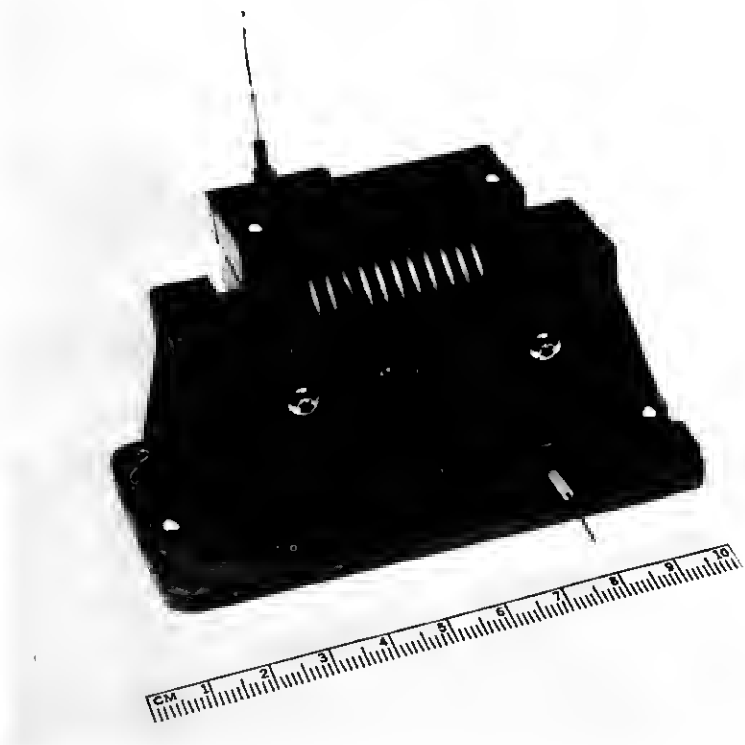

Fig. 18—The 2680A longitudinal choke.

quirements has resulted in the development of a special coaxial cable which comprises the winding and in the use of manganese-zinc ferrite core material. The compromise between permeability and coercive force appears to be appropriate.

7.2 Inductors

Eight inductor structures were developed and are shown in Fig. 19. Of the 68 codes using these designs, 27 are adjustable and form a stockpile of continuous inductance (0.0395 to 45 μH) for adjusting the mop-up filters. The remaining codes range up to 1000 μH. Wherever possible, designs have used the highly reliable procedures and materials developed for earlier systems. A new glass-bonded mica formulation with lower dielectric constant has been developed to lower distributed capacitance. New completely shielded designs have been necessary because of the tighter packing of components. Lower inductance units feature precisely spaced solenoidal windings, which are wound under tension and varnished in place. Higher inductance values are achieved by using varnish-coated, multiple-pie, duolateral windings.

The 1714A unit, shown in Figs. 19 and 20, is the most crucial inductor in the group. It measures 3.85 μH and is adjustable over a range of ± 2.5 percent. It is used to control repeater gain by varying β in the feedback amplifier. The length-to-diameter ratio is optimized to produce the

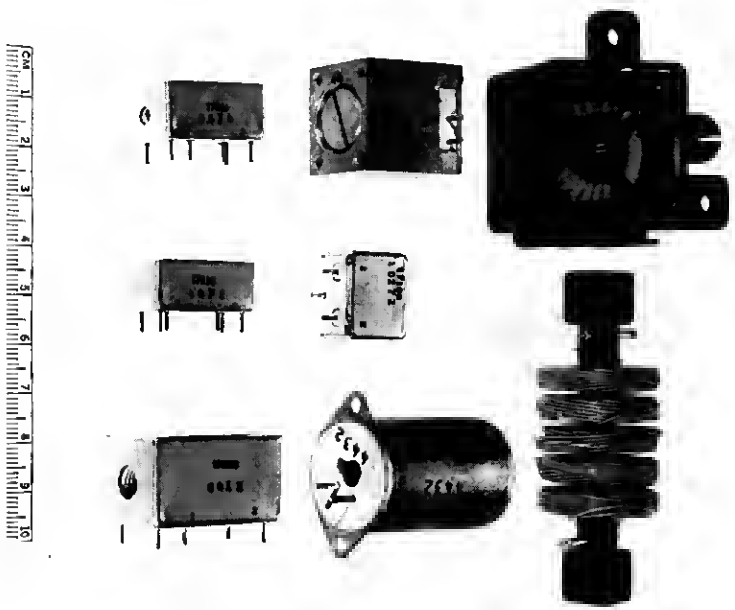

Fig. 19—Inductors.

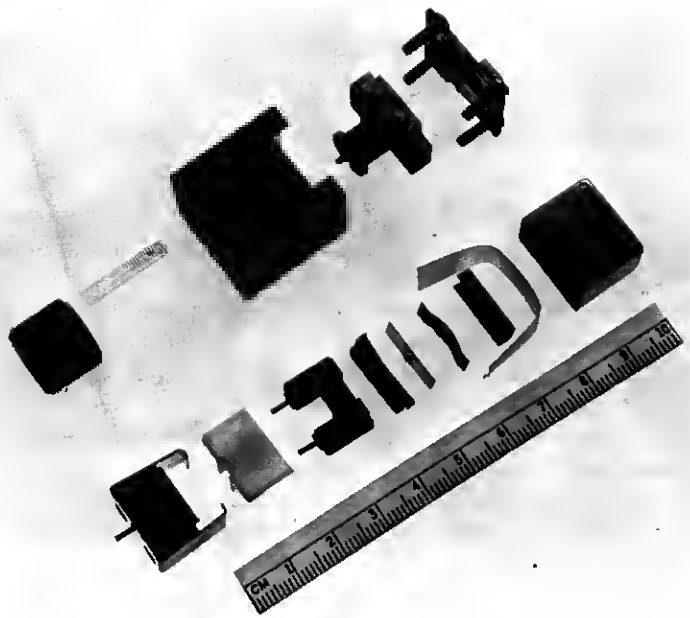

Fig. 20—Exploded view of 1710B and 1714A inductors.

highest possible principal resonance consistent with the attainment of high impedance at 200 MHz. Shielding is achieved by enclosing the winding in a brass block. Inductance is varied by turning a hollow brass plug in and out of the cavity to modify the inductor's magnetic field.

The 1710A and 1710B transistor feed chokes are 56 μH with ± 5 and ± 2 percent tolerances, respectively. Besides some initial adjustment capability, their first resonance (parallel resonance) must be at a high frequency and must exhibit high impedance. Also, the in-band third-harmonic products must not exceed -115 dBm when both fundamentals are at $+10$ dBm. These requirements have resulted in the design shown exploded in Fig. 20. The magnetic circuit consists of a small ferrite bar, separated from the ferrite winding spool by a mica shim to give a precise air gap. This ferrite bar is moved relative to the core to give the correct value of inductance. The position of the ferrite bar is maintained securely by spring-loaded clamps until the bar can be bonded in place.

The 1719A inductor shown in Fig. 19 is designed to produce 1 mH with the 0.657-A dc cable current through the winding. Because the unit must be corona-free to ground at 7,000 V dc, a magnetic core is not practical. As this inductor is in shunt with the signal path, it must maintain a specified minimum impedance up to 60 MHz. This is accomplished by winding the inductor as a duolateral coil of five sections. The *shunt* resonance (high impedance point) due to the overall inductance tuned by the effective capacitance is broad and occurs at 3 MHz. The first *series*

resonance due to magnetic coupling between the winding pies and the distributed capacitances occurs above 60 MHz, thus achieving the required minimum impedance of 1000 ohms over the band of interest.

7.3 Screening and reliability testing for transformers and inductors

To ensure that the inductive components would not be degraded after a long period of use, only materials were considered which had been thoroughly tested and which were determined to be suitable candidates for the proposed applications. All raw materials and piece parts were subjected to inspection, cleaning, and testing procedures before they were used. As a means of verifying and justifying the choice of material as well as methods of construction, all inductive components were subjected to artificial aging and stabilization.

This was accomplished by temperature cycling each component over the range from −18 to +66°C. The temperature cycles served two purposes: they accelerated aging changes and they established a trend line. Components were considered acceptable only if, after a series of temperature cycles, parameter changes were within permissible limits and the changes after each series of cycles were becoming smaller so that the extrapolated end-of-life changes would also be within the accepted limit.

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